REMARKS

Claims 2 and 8-34 are all the claims pending in the application.

Claims 2 and 8-34 are currently amended. Applicants respectfully submit that no new matter is added to currently amended claims 2 and 8-34. Claims 1 and 3-7 have been previously cancelled.

Claims 2 and 8-34 stand rejected under 35 U.S.C. §103(a) as unpatentable over U.S. Patent No. 6,487,699 to Devins in view of "An Embedded PowerPC SOC for Test and Measurement Applications." 13th Annual IEEE Int'l ASIC/SOC Conf. September 13-16, 2000, pp. 204-208 by Blaner et al., hereinafter, Blaner.

Applicants respectfully traverse the rejection based on the following discussion.

I. The 35 U.S.C. 103(a) Rejection as Unpatentable over Devins and Blaner

A. The Devins Reference

Devins discloses a method for controlling external models in a system-on-a-chip verification, in which an external memory-mapped test device (EMMTD) is coupled between a SOC design being tested in simulation, and cores external to the SOC design. The EMMTD is coupled to the SOC via a chip-external bus, and coupled to external cores, or to the external interfaces of cores internal to the SOC, via an EMMTD bi-directional bus. (col. 2, lines 36-42, which are cited by the Office Action).

Devins also discloses that a test case being executed for SOC verification by a simulated embedded processor in the SOC can communicate with and control elements external to the SOC, by using the EMMTD to perform such functions as initiating external core logic which drives test signals to an internal core, directly controlling an internal core via its external interface, or determining the states of an external core. (col. 3, lines 53-59).

Devins further discloses the EMMTD input connection 107 is connected to a chip-external bus, for example memory bus 2 as shown in Fig. 1. The bi-directional bus 207 of the EMMTD is represented by connections 104 and 105 to cores 106 and 108, respectively, corresponding to the example of Fig. 1. However, in general, the bi-directional bus 207 may be

as wide as desired; i.e., include as many wires as necessary to accommodate a desired number of cores to be communicated with/controlled. For each wire or bit on the bus, units 204, 205, 206, 207, 208 and 209 are replicated. (col. 3, lines 1-10, which are cited by the Office Action).

Devins also claims the element of "providing a hardware description language logic device coupled between said system-on-chip design and said external element," in independent claim 1, and similarly claims the "hardware description language logic device coupled between said system-on-chip design and said external element" in independent claims 12 and 23.

B. The Blaner Reference

Blaner discloses on page 205, cited by the Office Action, in II. SOC Structure, A. CPU and PLB [processor local bus] Subsystem, that "[t]he external bus interface unit (EBIU) controls up to eight banks of mixed types of memories and operates at one-half the PLB clock frequency. Either one of two banks may be used for non-volatile bootstrap memory. Further, the EBIU allows an off-chip device, called the external bus master, to take ownership of the external bus and access attached memories. (Page 205, 2nd full paragraph).

Blaner also discloses on page 208, IV. Design Verification, E. Verification Testbench, that "[b]ecause testcases are self-checking, all external activity is synchronized to the internal software. To accomplish this synchronization, a memory-mapped external device containing software readable and writable registers that appear as wires in the testbench is connected to the external bus. Verilog models accept the wires as triggers and respond with status on the wires." (Page 208, 2nd full paragraph).

C. Arguments

Currently amended, independent claim 2 recites in relevant part,

"a first external bus interface unit (EBIU) that is slaved to said master CPU; … a second EBIU connected to said first EBIU and to said verification interface model, wherein said test case software running on said master CPU controls both said SOC interface and said verification interface mode".

Similarly, currently amended, independent claim 8 recites in relevant part,

"a first external bus interface unit (EBIU) that is slaved and connected to said master CPU by a second internal bus; ... a second EBIU connected to said first EBIU by a second external bus and to said verification interface model by a third internal bus, wherein said test case software running on said master CPU controls both said SOC interface and said verification interface model".

Similarly, currently amended, independent claim 15 recites in relevant part,

"a first external bus interface unit (EBIU) that is slaved and connected to said master CPU by a second internal bus; ... a second EBIU connected to said first EBIU by a second external bus and to said verification interface model by a third internal bus, wherein said second EBIU and said first EBIU are mastered by said master CPU of said SOC, such that, said SOC interface and said verification interface model are programmed by said test case software running on said master CPU".

Similarly, currently amended, independent claims 21 and 28 recite in relevant part,

"slaving an SOC interface and a first external bus interface unit (EBIU) of said SOC to a master CPU of said SOC; ... connecting said first EBIU to a second EBIU, which is external to said SOC, said second EBIU connecting to said external verification interface model; and controlling both said SOC interface of said SOC and said external verification interface model by test case software running on said master CPU of said SOC".

Devins merely discloses that an SOC design can be verified by running a test case on a simulated processor of the SOC and that an external memory-mapped test device (EMMTD), which may be a hardware description language logic device, controls an external core in response to the test case being executed by the simulated processor of the SOC. The EMMTD is merely coupled to the simulated processor of the SOC running the test case by an external bus interface logic (EBIU).

In contrast, Applicants respectfully submit that the present invention does not contain external structures analogous to the external core(s) or external core drivers of Devins. Instead, as is obvious to one of ordinary skill in the art, the "external cores" of Devins correspond to the present invention's internal cores of the SOC that are run by test case software on the master

CPU of the SOC, not a simulation of the processor as in Devins. Internal cores of the present invention are verified by test patterns run by the master CPU of the SOC and are communicated to the first EBIU of the SOC and thence, to the second EBIU of the external verification test bench, all under the control of the master CPU, to program (by software drivers provided by the master CPU) the external verification interface model, so that its interface may be compared to the SOC interface, which is also controlled by the master CPU running the test cast software.

In addition, Applicants respectfully submit that the present invention does not contain a structure analogous to the EMMTD of Devins. Because the external cores and the simulated processor of Devins are external to both the EMMTD and the SOC of Devins, Devins requires a logic/mapping device to receive the simulated processor's instructions for the external core and to process and send these instructions to the external cores.

In contrast, Applicants respectfully submit that because the processor, i.e., the master CPU, and the internal cores of the present invention are internal to the SOC, only an external verification interface model need be programmed to compare its interface with that of the SOC interface to verify test case software run by the master CPU of the SOC.

Furthermore, the present invention comprises two EBIUs, one EBIU internal to the SOC, and the second EBIU external to the SOC and residing on the external verification test bench.

For at least the reasons outlined above, Applicants respectfully submit that Devins does not disclose, teach or suggest the features of: "a first external bus interface unit (EBIU) that is slaved to said master CPU; ... a second EBIU connected to said first EBIU and to said verification interface model, wherein said test case software running on said master CPU controls both said SOC interface and said verification interface mode", as recited in currently amended, independent claim 2; "a first external bus interface unit (EBIU) that is slaved and connected to said master CPU by a second internal bus; ... a second EBIU connected to said first EBIU by a second external bus and to said verification interface model by a third internal bus, wherein said test case software running on said master CPU controls both said SOC interface and said verification interface model", as recited in currently amended, independent claim 8; "a first external bus interface unit (EBIU) that is slaved and connected to said master CPU by a second internal bus; ... a second EBIU connected to said first EBIU by a second external bus and to said

verification interface model by a third internal bus, wherein said second EBIU and said first EBIU are mastered by said master CPU of said SOC, such that, said SOC interface and said verification interface model are programmed by said test case software running on said master CPU", as recited in currently amended, independent claim 15; "slaving an SOC interface and a first external bus interface unit (EBIU) of said SOC to a master CPU of said SOC; ... connecting said first EBIU to a second EBIU, which is external to said SOC, said second EBIU connecting to said external verification interface model; and controlling both said SOC interface of said SOC and said external verification interface model by test case software running on said master CPU of said SOC", as recited in currently amended, independent claims 21 and 28.

The Office Action asserts that "Blaner, on the other hand, does expressly teach the existence of an SOC EBIU ("External Bus Interface Unit"). Blaner shows an EBIU in the extreme upper-left hand corner of the SOC block diagram (See Blaner: Fig. 2 and p. 205). This diagram shows that the SOC EBIU connects externally to "SRAM, Flash, ROM, or an External Master". Examiner interprets the 'External Master' as corresponding to the EMMTD taught in Devins. (Office Action, page 5, printed lines 9-14).

Blaner discloses on page 205, cited by the Office Action, in II. SOC Structure, A. CPU and PLB [processor local bus] Subsystem, that "[t]he external bus interface unit (EBIU) controls up to eight banks of mixed types of memories and operates at one-half the PLB clock frequency. Either one of two banks may be used for non-volatile bootstrap memory. Further, the EBIU allows an off-chip device, called the external bus master, to take ownership of the external bus and access attached memories. (Page 205, 2nd full paragraph).

Blaner also discloses on page 208, IV. Design Verification, E. Verification Testbench, that "[b]ecause testcases are self-checking, all external activity is synchronized to the internal software. To accomplish this synchronization, a memory-mapped external device containing software readable and writable registers that appear as wires in the testbench is connected to the external bus. Verilog models accept the wires as triggers and respond with status on the wires." (Page 208, 2nd full paragraph).

Blaner does not cure the deficiencies of Devins.

Applicants respectfully submit that the Office Action is in error, when it interprets the 'External Master' of Blaner as corresponding to the External Memory-Mapped Test Device (EMMTD) of Devins or the EMMTD described by Blaner.

The external master bus of Blaner is an off-SOC device that merely takes ownership of the external bus to access memory units that are attached to the external bus. (Page 205, 2nd full paragraph).

On the other hand, the EMMTD of Devins is a logic/mapping device that receives the simulated SOC's processor's instructions for an external core, and processes and sends these instructions to the external core. Thus, the actions of Devin's EMMTD are synchronized to the running of the simulated SOC's processor. A point that is further strengthened by Blaner's description of "[b]ecause testcases are self-checking, all external activity is synchronized to the internal software. To accomplish this synchronization, a memory-mapped external device containing software readable and writable registers that appear as wires in the testbench is connected to the external bus." (emphasis added).

Nowhere does Blaner disclose, teach or suggest that the "External Master' is synchronized to the internal software of the SOC's simulated processor, as is the EMMTD of Devins. Instead, Blaner merely discloses that "the EBIU allows an off-chip device, called the external bus master, to take ownership of the external bus and access attached memories." (Page 205, 2nd full paragraph).

For at least the reasons outlined above, Applicants respectfully submit that the Office Action incorrectly analogizes the 'External Master' of Blaner to the MMTD of Devins.

Furthermore, nowhere does Blaner disclose, teach or suggest the present invention's features of disclose, teach or suggest the features of: "a first external bus interface unit (EBIU) that is slaved to said master CPU; … a second EBIU connected to said first EBIU and to said verification interface model, wherein said test case software running on said master CPU controls both said SOC interface and said verification interface mode", as recited in currently amended, independent claim 2; "a first external bus interface unit (EBIU) that is slaved and connected to said master CPU by a second internal bus; … a second EBIU connected to said first EBIU by a second external bus and to said verification interface model by a third internal bus,

wherein said test case software running on said master CPU controls both said SOC interface and said verification interface model", as recited in currently amended, independent claim 8; "a first external bus interface unit (EBIU) that is slaved and connected to said master CPU by a second internal bus; … a second EBIU connected to said first EBIU by a second external bus and to said verification interface model by a third internal bus, wherein said second EBIU and said first EBIU are mastered by said master CPU of said SOC, such that, said SOC interface and said verification interface model are programmed by said test case software running on said master CPU", as recited in currently amended, independent claim 15; "slaving an SOC interface and a first external bus interface unit (EBIU) of said SOC to a master CPU of said SOC; … connecting said first EBIU to a second EBIU, which is external to said SOC, said second EBIU connecting to said external verification interface model; and controlling both said SOC interface of said SOC and said external verification interface model by test case software running on said master CPU of said SOC", as recited in currently amended, independent claims 21 and 28. Instead, Blaner merely discloses that "the EBIU allows an off-chip device, called the external bus master, to take ownership of the external bus and access attached memories."

For at least the reasons outlined immediately above in regard to Blaner and to those reasons outlined above in regard to Devins, Applicants respectfully submit that Devins and Blaner, either individually or in combination, do not disclose, teach or suggest the present invention's features of: "a first external bus interface unit (EBIU) that is slaved to said master CPU; … a second EBIU connected to said first EBIU and to said verification interface model, wherein said test case software running on said master CPU controls both said SOC interface and said verification interface mode", as recited in currently amended, independent claim 2; "a first external bus interface unit (EBIU) that is slaved and connected to said master CPU by a second internal bus; … a second EBIU connected to said first EBIU by a second external bus and to said verification interface model by a third internal bus, wherein said test case software running on said master CPU controls both said SOC interface and said verification interface model", as recited in currently amended, independent claim 8; "a first external bus interface unit (EBIU) that is slaved and connected to said master CPU by a second internal bus; … a second EBIU connected to said first EBIU by a second external bus and to said verification interface model by

a third internal bus, wherein said second EBIU and said first EBIU are mastered by said master CPU of said SOC, such that, said SOC interface and said verification interface model are programmed by said test case software running on said master CPU", as recited in currently amended, independent claim 15; "slaving an SOC interface and a first external bus interface unit (EBIU) of said SOC to a master CPU of said SOC; … connecting said first EBIU to a second EBIU, which is external to said SOC, said second EBIU connecting to said external verification interface model; and controlling both said SOC interface of said SOC and said external verification interface model by test case software running on said master CPU of said SOC", as recited in currently amended, independent claims 21 and 28. Accordingly, Devins and Blaner, either individually or in combination, fail to render obvious the subject matter of currently amended, independent claims 2, 8, 15, 21, and 28, and dependent claims 9-14, 16-20, 22-27, and 29-34 under 35 U.S.C. §103(a). Withdrawal of the rejection of claims 2 and 8-34 under 35 U.S.C. §103(a) as unpatentable over Devins and Blaner is respectfully solicited.

II. Formal Matters and Conclusion

Claims 2 and 8-34 are pending in the application.

With respect to the rejection of the claims over the cited prior art, Applicants respectfully argue that the currently amended claims are distinguishable over the prior art of record. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections to the claims.

In view of the foregoing, Applicants submit that claims 2 and 8-34, all the claims presently pending in the application, are patentably distinct from the prior art of records and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest time possible.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

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